

10. (Thrice Amended) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a plurality of pixel electrodes formed in a plurality of pixel areas decided by the gate wirings and the data wirings and arranged in a matrix shape;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers having impurity formed on both sides of the operating semiconductor layer, a source electrode including the first semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer and the gate electrode; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the

20 second storage capacitor electrode, and a second storage capacitor is structured by the second  
21 storage capacitor electrode, the second insulating film and the pixel electrode.

1 11. (Amended) An active matrix type display comprising:  
2 a plurality of gate wirings formed on a substrate;  
3 a plurality of data wirings formed on the substrate substantially orthogonal to  
4 the gate wirings;  
5 a plurality of pixel electrodes formed in a plurality of pixel areas decided by the  
6 gate wirings and the data wirings and arranged in a matrix shape;  
7 a thin film transistor formed in each of the pixel areas and structured planar  
8 type having an operating semiconductor layer formed on the substrate, a gate insulating film  
9 formed on the operating semiconductor layer, a gate electrode formed on the gate insulating  
10 film and connected to one of the gate wirings, first and second semiconductor layers formed  
11 on both sides of the operating semiconductor layer, a source electrode including the first  
12 semiconductor layer electrically connected to the pixel electrode via a contact window  
13 opened to first and second insulating layers laminated on the first semiconductor and the gate  
14 electrode;  
15 an impurity semiconductor layer formed isolated from the first semiconductor  
16 layer on the substrate and made of the same material as the first semiconductor layer; and  
17

18 a plurality of storage capacitor electrodes using the first semiconductor layer as  
19 a first storage capacitor electrode, having a second storage capacitor electrode being formed  
20 between the first insulating film and the second insulating film and connected to a storage  
21 capacitor wiring maintained at a predetermined potential, wherein at least a first storage  
22 capacitor is structured by the first storage capacitor electrode, the first insulating film and the  
23 second storage capacitor electrode, and a second storage capacitor is structured by the second  
24 storage capacitor electrode, the second insulating film and the pixel electrode.

1 12. (Amended) An active matrix type display comprising:  
2 a plurality of gate wirings formed on a substrate;  
3 a plurality of data wirings formed on the substrate substantially orthogonal to  
4 the gate wirings;  
5 a first, a second and a third insulating film formed on the gate wirings;  
6 a pixel electrode formed in a pixel decided by the gate wirings and the data wirings:  
7 a thin film transistor formed in the pixel and having a gate electrode connected  
8 to one of the gat wirings, a source electrode connected to the pixel electrode, and a drain  
9 electrode connected to the data wirings;  
10 a first storage capacitor electrode formed between the first insulating film and  
11 the second insulating film in an area of the gate wiring for previous pixel to the pixel and  
12 connected to the pixel electrode; and

13 second storage capacitor electrode also serving as a storage capacitor wiring  
14 formed between the second insulating film and the third insulating film in the area of the gate  
15 wiring;

16 wherein a first storage capacitor is structured by the first storage capacitor  
17 electrode, the second insulating film and the second storage capacitor electrode, and a second  
18 storage capacitor is structured by the second storage capacitor electrode, the third insulating  
19 film and the pixel electrode.

1 13. (Amended) An active matrix type display as set forth in claim  
2 12, wherein a third storage capacitor is structured by the first storage capacitor electrode, the  
3 first insulating film and the gate wiring.

1 15. (Amended) An active matrix type display as set forth in claim  
2 12, wherein the second storage capacitor electrode also serves as a shading film.

#### REMARKS

Claim 10 stands rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al. (U.S. 6,317,173). Applicants respectfully traverse this rejection because the cited reference does not disclose (or suggest) a semiconductor layer having impurity being used as a storage capacitor electrode, as in claim 10 of the present invention, as amended.